Colloidal quantum dot field-effect transistors

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3. An All-solution-based Hybrid CMOS-like Quantum Dot/Carbon Nanotube Inverter*

The development of low-cost, flexible electronic devices is subordinated to the advancement in solution-based and low-temperature-processable semiconducting materials, such as colloidal quantum dots (QDs) and single-walled carbon nanotubes (SWCNTs). Here we demonstrate excellent compatibility of QDs and SWCNTs as a complementary pair of semiconducting materials for the fabrication of high-performance CMOS-like inverters. The n-type FETs based on I^- capped PbS QDs (V_{th}= 0.2 V, On/Off = 10^5, S_{S-th}= 114 mV/dec, μ_e= 0.22 $cm^2V^{-1}s^{-1}$) and the p-type FETs with tailored parameters based on low density random network of SWCNTs (V_{th}= -0.2 V, On/Off > 10^5, S_{S-th}= 63 mV/dec, μ_h= 0.04 $cm^2V^{-1}s^{-1}$) were integrated on the same substrate in order to obtain high performance hybrid inverters. The inverters operate in the sub-1Volt range (0.9 V) and have high gain (76 V/V), large maximum-equal-criteria noise margins (80%) and peak DC power consumption of 3 nW, in combination with low hysteresis (10 mV).

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3.1. Introduction

Solution processable electronic materials are in great demand since they can be applied in low-cost, flexible electronic devices and circuits. Among the materials, which have attracted the most attention, are single-walled carbon nanotubes (SWCNTs) and colloidal quantum dots (QDs).

Over the last few years, QDs have been used to fabricate solar cells, LEDs, displays, near-infrared photodetectors, and microelectronic circuits.[1-10] PbS and CdSe QDs have been the most studied; however, their applicability in electronics is hampered by the difficulty in achieving unipolar p-type charge transport and high device stability. On the other hand, SWCNTs have been implemented in radio frequency identification tags, sensors, memories, and digital circuits.[11-17] In its turn, the continuous, stable, and reliable n-type doping of SWCNTs still remains challenging, limiting the performance of SWCNT-based electronics.

Both CdSe QDs (as n-type material) and SWCNTs (as p-type material) FETs were reported as building blocks of unipolar logic devices (e.g. inverters).[8,10,18,19] The unipolar logic, in theory, features lower noise margin (that is a figure of merit of the stability of the logic circuit to a voltage noise) and higher power consumption in respect to CMOS or even ambipolar (CMOS-like) logic devices.[20,21] As a possible improvement on unipolar inverters, ambipolar devices based on PbS QDs or nanotubes FETs were reported.[9,22] However, the low band-gap in ambipolar, often partially-sintered PbS QDs films results in a high “off” current of the transistors, thereby increasing the power consumption and affecting the noise margins of the inverter. SWCNTs, similarly, have been utilized in doping-free ambipolar inverters.[23-25] Various strategies have been applied to obtain n-doped SWCNTs for the fabrication of CMOS-like inverters.[26-31] Since reliable, stable, and tunable n-doping of SWCNTs still remains challenging, hybrid inverters, which combine a complementary pair of semiconductors as SWCNTs with an n-type material, such as MoS_2, IGZO, IZO or ZTO, have been reported.[32-36] Although the reported inverters operate successfully, their performance in terms of noise margins and power consumption leaves much to be desired.

In the case of the QDs, to the best of our knowledge, the hybrid approach for the fabrication of CMOS-like inverters was not attempted yet. Stable, solution-based, unipolar FETs with well-controlled threshold voltage, low hysteresis, and high mobility are in high demand for fabrication of high-noise-margins, low-voltage, and low-power-consumption inverters and other logic elements.

Here we report a hybrid CMOS-like inverter, integrated on a single glass substrate, based on all-solution-based FETs gated with a high capacitance (157 nF·cm^{-2}) P(VDF-TrFE-CFE)/PMMA polymer dielectric layer. The n-type FETs are made of I$^-$ capped PbS QDs and show an on-off ratio of 10^5, a subthreshold swing of 114 mV per decade, a threshold voltage of 0.2 V, a hysteresis of 20 mV, and electron mobility of 0.22 cm^{2}V^{-1}s^{-1}. The p-type transistor is based on a low-density random network of polymer-selected semiconducting SWCNTs and features an on-off ratio of 10^5, a subthreshold swing of 63 mV per decade, a threshold voltage of -0.2 V, a hysteresis of 20mV, and a linear mobility of 0.04 cm^{2}V^{-1}s^{-1}. The CMOS-like inverter operates in sub-1V voltage range (power supply voltage of 0.9 V), and shows high static gain (76 V/V), large noise margins (80%), and small hysteresis (10 mV), with the peak DC power consumption of 3 nW, which are the best reported values for all-solution-processable inverters to date.

3.2. Results and discussion

As it was reported earlier, P(VDF-TrFE-CFE) is a good gate dielectric material for solution-processable FETs based on SWCNTs, QDs, and organic semiconductors.[37-39] Since P(VDF-TrFE-CFE) does not contain electron trapping groups and can encapsulate the active layer, protecting it from water and oxygen, this polymer is especially interesting as a gate material for n-type FETs. However, when P(VDF-TrFE-CFE) is used as gate dielectric several challenges appear as the difficulty to obtain continuous and smooth layers and the hysteresis loop in the transfer curves, which can be explained by its relaxor ferroelectric nature.[38] To decrease the hysteresis, and increase the reproducibility of the device fabrication, in this work we used on top of the P(VDF-TrFE-CFE) film a thin film of amorphous poly(methyl methacrylate) (PMMA). PMMA is a low-dielectric-constant “passive” layer in series

with the relaxor ferroelectric P(VDF-TrFE-CFE), thus the addition of the PMMA reduces the ferroelectric properties and the dielectric constant of the combined dielectric layer (see the discussion in Appendix, Figure 3.A1).[40]

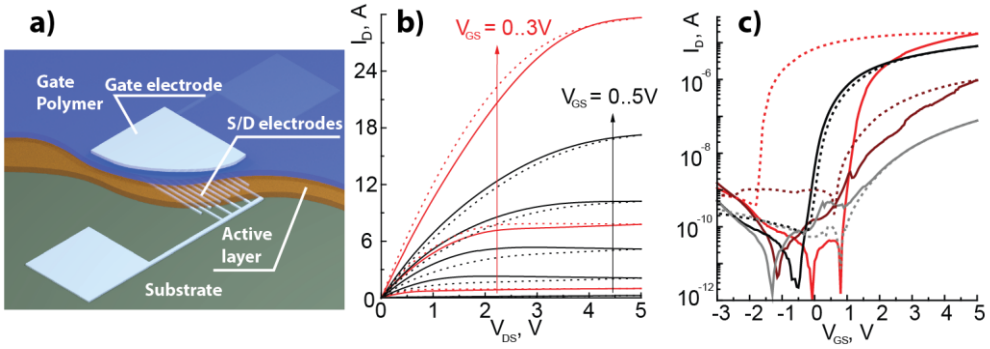


Figure 3.1. *Comparison of P(VDF-TrFE-CFE) /PMMA and P(VDF-TrFE-CFE) as gate dielectrics for I- capped PbS QDs FETs.* ***a)*** *Schematic structure of the device.* ***b)*** *Comparison of the output characteristics of I- capped FETs with P(VDF-TrFE-CFE) (V_{GS} = 0..3V, ΔV_{GS} = 1V, red curves) and P(VDF-TrFE-CFE) /PMMA (V_{GS} = 0..5V, ΔV_{GS} = 1V, black curves). The arrows indicate increasing of V_{GS}.* ***c)*** *Comparison of the transfer characteristics of I- capped FETs with P(VDF-TrFE-CFE) (red curve) and P(VDF-TrFE-CFE)/PMMA (black curve) gate dielectrics with corresponding gate leakages (dark red and gray curves, respectively) for V_{DS} =1V. Dotted curves represent the reverse hysteresis branches.*

As first the difference between P(VDF-TrFE-CFE)-only and P(VDF-TrFE-CFE)/PMMA as gate dielectric layers in I- capped PbS QDs FETs is investigated, the device structure used is displayed schematically in Figure 3.1a. Almost pure n-type charge transport in the PbS QDs transistor is achieved, as it is demonstrated by the output curves shown in Figure 3.1b. This is obtained using a low-work-function metal such as Ag for the fabrication of source and drain electrodes, lithographically patterned on n++ Si/SiO^2 substrate, that blocks holes and favors electron injection. Before deposition of the active material, the substrate is annealed in an N_2 filled glovebox in order to desorb oxygen and water from the SiO_2 surface. After depositing the I- capped PbS QDs film, the P(VDF-TrFE-CFE) or P(VDF-TrFE-CFE)/PMMA top gate was spin-coated as schematically indicated in Figure 3.1a.

The electron saturation current measured for the same gate voltage is higher for P(VDF-TrFE-CFE) -gated devices than for the P(VDF-TrFE-CFE)/PMMA-gated ones, due to higher gate capacitance of the first (204 $nF \cdot cm^{-2}$ (k = 46)) respect to the second gate (157 $nF \cdot cm^{-2}$ (k = 35)). It is also important to note that the two types of transistors exhibit different shifts of the threshold voltage due to the different ferroelectric properties of the two gates. The small hysteresis in the output curves displayed in Figure 3.1b (the dashed curves show the reverse voltage sweep) indicates a low charge trapping rate in the film and at the interfaces, which is a nontrivial achievement in quantum dot FETs. The different hysteresis shape indicates dissimilar underlying processes in P(VDF-TrFE-CFE) and P(VDF-TrFE-CFE)/PMMA-gated FETs; in case of P(VDF-TrFE-CFE)/PMMA, the reverse sweep current is lower than the forward sweep because of charge trapping, probably caused by defects formed at the QD surface during the ligand-exchange process, which is a frequently reported mechanism in PbS QDs FETs. In case of P(VDF-TrFE-CFE), the reverse current is higher, most probably because of the remnant polarization of the gate dielectric in the region close to the source/drain electrodes due to the polarization of the gate electrode across the channel, that overcomes the current decrease due to the charge trapping process.

This effect is even more visible in the transfer curves (Figure 3.1c). The sweep of the gate voltage polarizes the gate and the difference in the remnant polarization causes strong differences in the hysteresis magnitude and shape. For P(VDF-TrFE-CFE)/PMMA, the hysteresis is only 0.17V, which to the best of our knowledge, is the smallest reported value for PbS QDs FETs; for P(VDF-TrFE-CFE) the hysteresis is significantly larger (2.7 V) and the reverse current is higher than the forward one, showing a similar behavior as in the output curves. Because of the relaxor ferroelectric nature of P(VDF-TrFE-CFE), the remnant polarization is not stable and decays within minutes resulting in a decay of the drain current after applying a gate voltage pulse to the FET (see Appendix, Figure 3.A2). Although the gate leakage current for P(VDF-TrFE-CFE) (dark red curve in Figure 3.1c) is almost one order of magnitude higher than the leakage through P(VDF-TrFE-CFE)/PMMA (gray curve in Figure 3.1c), the gate leakages varies for FETs and over multiple devices providing no strong evidence that the P(VDF-TrFE-CFE)/PMMA insulates the gate electrode better than the P(VDF-TrFE-CFE). In the device configuration used in this work, the gate electrode is not patterned and the overlap of the gate and source/drain electrodes is quite high,

thus increasing the possibility of a defect leading to a direct leakage from the gate to the source or drain electrodes. Additionally, the contact probes can easily penetrate the gate electrode metal and the gate dielectric, during the measurement of the devices, causing a current leakage through the active layer, proportional to the applied source/gate voltage difference. Here it is also important to notice that the P(VDF-TrFE-CFE)/PMMA gate encapsulates the active layer making these devices stable for several months in an N_2-filled glovebox and for several hour exposure to air, with no clear change in the threshold voltage, electron mobility or on-off ratio.

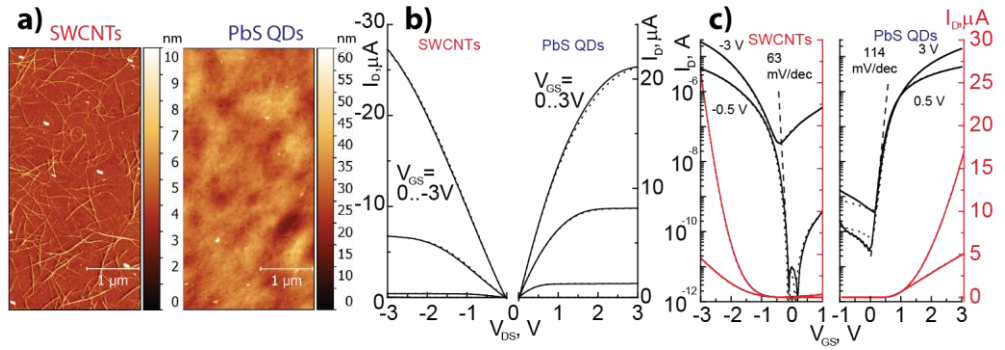


Figure 3.2. *Complementary SWCNTs and I- capped PbS QDs FETs with the P(VDF-TrFE-CFE)/PMMA gate dielectric integrated on a glass substrate.* ***a)*** *AFM images of SWCNTs random network and PbS QDs thin film (120 nm).* ***b)*** *Output characteristics of SWCNT (left) and I- capped PbS QDs (right) FETs.* ***c)*** *Transfer curves of SWCNTs (left) and I- capped PbS QDs (right) FETs in logarithmic (black) and linear (red) scale for V_{DS} = 0.5V (linear regime) and 3V (saturation regime). The dashed lines indicate subthreshold swing, dotted curves are reverse hysteresis branches.*

Figure 3.2 shows the complementary pair of FETs integrated on the single glass substrate. After cleaning and annealing the glass substrate similarly to the Si/SiO_2 substrate described above, the PbS QDs film was spin-coated onto one part of the substrate and the SWCNTs random network was deposited, using a blade coating technique, on the opposite part. The morphology of the two layers is shown by the atomic force microscopy (AFM) micrographs reported in Figure 3.2a. Subsequently, the P(VDF-TrFE-CFE) and PMMA polymer layers were spin-casted on the whole substrate and the gate electrodes were evaporated through a shadow mask. Figure 3.2a and 3.2b show output and transfer curves of the SWCNTs FET (left) and the PbS

QDs FET (right), respectively. The channel geometries were selected to achieve a complementary pair of FETs with appropriate threshold voltages and linear/saturation current. The linear and the saturation electron mobilities of the PbS QDs film, extracted from V_{DS} = 1V and V_{DS} = 5V transfer curve for the FET with the channel length of 30 μm and the channel width of 5 mm (see Appendix, Figure 3.A4, 3.A5, and Table 3.A1), have values of about 0.22 $cm^2V^{-1}s^{-1}$. Furthermore, the contact-resistance correction obtained analyzing transistors with channel lengths 5, 10, 20, 30 and 40 μm confirms the above linear mobility value (Appendix Table 3.A2). This electron mobility, in combination with the low hysteresis, the subthreshold swing of 114 mV/decade, the on-off ratio of 10^5, and the threshold voltage of 0.2 V characterize the P(VDF-TrFE-CFE)/PMMA gated PbS QDs FETs as a suitable n-type component for low cost and low voltage electronics. The off current is limited by the intrinsic ambipolarity and relatively low band gap of PbS QDs explaining the minor injection of holes in the channel even from the low-work-function electrodes. The optical absorbance measurements (Appendix Figure 3.A3) show that the ligand exchange and annealing do not cause significant sintering of I^- capped PbS QDs film; therefore, the quantum confinement of the individual quantum dots is not compromised enabling high on-off ratio and low subthreshold swing.

As mentioned, a low-density semiconducting SWCNTs random network (see the AFM image in Figure 3.2a, left) was deposited since the hole mobility of a high-density network can be orders of magnitude higher than the electron mobility of PbS QDs.[41] Additionally, increasing the number of intertube crossings in the current pathway can be considered as a contact resistance that increases with the channel length.[42] Therefore, the correction of the mobility for the channel-length-independent contact resistance, made for PbS QDs film, cannot be implemented for the SWCNTs low-density random network. Additionally, using the geometrical size of the channel in the calculations leads to the underestimation of the mobility: the actual channel width for the current pathway is strongly overestimated since the current pathway takes place through individual carbon nanotubes and not through the geometrical channel width; the actual channel length is underestimated, since the current pathway goes through interconnected carbon nanotubes, which is significantly larger than the direct distance between the patterned electrodes. Without any corrections, the linear and the saturation hole mobility extracted for the device with 10 μm channel, presented in Figure 3.2, are, 0.04 and 0.09 $cm^2V^{-1}s^{-1}$, respectively.

The value of linear hole mobility is more than twice lower than the saturation mobility enforcing our assumption that the linear current has been influenced by the contact resistance. A minor electron current is observed in the transfer curves because of intrinsic nature of SWCNTs purified with the polyfluorene derivative poly(9,9-di-n-dodecylfluorenyl-2,7-diyl) (PF-12) polymer, which for higher source-drain voltages affects the off-state of the FET.[43] However, for low voltage operation (V_{DS} = 0.5 V), the device showed an on-off ratio higher than 10^5, very low subthreshold swing of 63 mV/decade (which is only slightly higher than the theoretical limit of 60 mV/decade for 300 K) and a threshold voltage of -0.2 V.

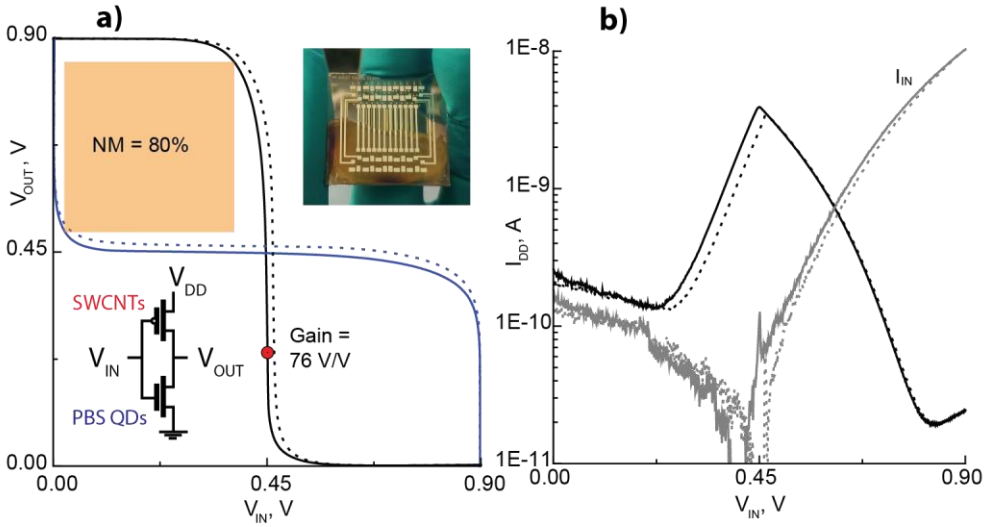


Figure 3.3. *Hybrid CMOS-like PbS QDs/SWCNTs inverter.* ***a)*** *The direct (black) and mirrored (blue) VTC of the inverter for V_{DD} = 0.9 V. Inset – a photograph of the substrate and schematic connection of the inverter. The orange square indicates static noise margins determined according to the maximum equal criteria principle.* ***c)*** *The current through the "V_{DD}" terminal (black) with an indication of the current through the "V_{IN}" terminal (gray). Dotted curves are the reverse hysteresis branches.*

Figure 3.3 shows the performance of the CMOS-like inverter based on P(VDF-TrFE-CFE)/PMMA gated p-type SWCNTs and n-type PbS QDs FETs. The inverter was characterized using 6 probes, connecting the complementary pair of FETs to the measuring setup according to the schematics in the inset of Figure 3.3a. The voltage transfer curve (VTC) of the inverter, operating for V_{DD} = 0.9V, is shown in Figure 3.3a for the forward (solid black curve) and reverse (dashed black curve) sweep. The static

gain reaches a maximum value of 76 V/V for V_{IN} = 0.45V. For the high-output state of the inverter (V_{IN} = 0 V), the output voltage is 99.77% of V_{DD}, and for the low-output state (V_{IN} = 0.9 V), it is 0.31% of V_{DD}. The mirrored VTC (blue solid and dashed lines for forward and reverse hysteresis, respectively) is shown in order to illustrate the noise margins of 80%, determined accordingly to the "maximum equal criteria" principle for the forward sweep curve.[21,44] The current, measured through the power supply (black curve, I_{DD}) and input (gray curve, I_{IN}) terminals are plotted in Figure 3.3b. The VTC hysteresis of 10mV is caused by the PbS QDs FET, which follows from the hysteresis shape of the current measurements. The I_{DD} is 0.2 nA (in the high-output state) and 25 pA (in the low-output state), which are limited respectively by the gate leakage current in the PbS QDs FET and by the minor electron current through the SWCNTs FET. The I_{IN} is determined by the gate leakages and is ~0.1 nA for the high-output state (gate leakage through the SWCNTs FET) and is growing up to 10 nA for the low-output state (gate leakage through the PbS QDs FET). The maximum DC power consumption of the inverter occurs in the switching point and is 3 nW. Therefore, to the best of our knowledge, this hybrid inverter shows the highest reported static gain and noise margins for transistors made with fully solution processable materials.

As for reproducibility of our results, since the mobility of SWCNTs random network depends strongly on the density, the switching voltage (the noise margins) and the gain value varied slightly for different samples. FETs made from high-density SWCNTs network showed hole mobility of 0.9 $cm^2V^{-1}s^{-1}$; however, the gate leakage current increased proportionally and influenced the VTC curves of the inverters. Although the inverters showed high performance with the noise margins up to 84% (for V_{DD} = 2V) and the gain up to 220 V/V (for V_{DD} = 3V), the steady-state power consumption increased because of the gate leakage and electron current for higher power supply voltages in the SWCNTs FETs.

3.3. Conclusions

In conclusion, we show that PbS QDs film and SWCNTs random network can be used as a complementary pair of materials for fabrication of high-performance all-

solution-processable CMOS-like inverters, build up from high-*k*-polymer-gated FETs. The n-type FET shows an on-off ratio of 10^5, a subthreshold swing of 114 mV per decade, a threshold voltage of 0.2 V, a hysteresis of 20 mV, and electron mobility of 0.22 $cm^2V^{-1}s^{-1}$. Silver electrodes in combination with I^- ligands determine an almost perfect unipolar n-type charge transport through PbS QDs film. A low-density network of SWCNTs was used in order to get complementary charge transfer characteristics to the n-type PbS QDs FET. The p-type SWCNTs FETs display an on-off ratio higher than 10^6, a subthreshold swing of 63 mV per decade, a threshold voltage of -0.2 V, a hysteresis of 20mV, and a linear mobility of 0.04 $cm^2V^{-1}s^{-1}$. The reported inverter features sub-1V operation (V_{DD} = 0.9 V) with the highest reported static gain (76 V/V) and noise margins (80 %) for fully solution processable devices, to the best of our knowledge. It should be noted that the high-*k* gate dielectric P(VDF-TrFE-CFE)/PMMA (*k* = 35) can be used in low-voltage, low-hysteresis FETs providing a gate capacitance of 157 $nF \cdot cm^{-2}$ and serves also as an encapsulating layer for air-sensitive materials.

As future perspective, ample room is available for further improving the performance, reproducibility, and fabrication process of these inverters. Firstly, using a patterned gate electrode would improve the frequency response of the logic device. Secondly, recent developments in PbS QDs inks based on solution-phase ligand exchange may allow switching to a single step printing technique, for which SWCNTs have been demonstrated to be fully compatible. [25,47,48] Furthermore, robust self-assembly of SWCNTs was recently reported in FETs, a technique that could be used for the fabrication of integrated inverters with SWCNTs and PbS QDs. [49]

3.4. Experimental details

PbS QDs synthesis. Materials: Lead (II) acetate trihydrate ($Pb(CH_3COO)_2 \times 3H_2O$, ≥ 99.99%, Aldrich), bis(trimethylsilyl)sulfide (TMS_2S, Aldrich), 1-octadecene (ODE, 90%, Aldrich), oleic acid (OA, 90%, Aldrich), ethanol (Fluka), hexane (Aldrich), tetrachloroethylene (TCE, 99%, Aldrich) were used as received.

3.2 nm PbS QDs were synthesized according to the method of Hines et al. with slight modifications.[45] $Pb(CH_3COO)_2 \times 3H_2O$ (1.5 g, 4 mmol), ODE (47.2 mL) and oleic acid (2.8 mL) were mixed in a three-neck flask. The mixture was degassed under vacuum at 120°C for 1 hour. Then the temperature was adjusted to 95 °C under argon flow. The heating mantle was removed and solution of TMS_2S (0.42 mL, 2 mmol) in 10 mL ODE (dried) was injected into vigorously stirring lead oleate solution. After 5 min, the reaction mixture was cooled down to room temperature by ice bath. QDs were washed three times with toluene/ethanol solvent/nonsolvent pair (1st washing: 30 mL hexane/120 mL ethanol; 2nd washing: 30/36; 3rd washing: 15/16), redissolved in 7 mL hexane and filtered through 0.2 μm PTFE filter.

Preparation and characterization of semiconducting SWCNTs dispersion. HiPco SWCNTs (0.8-1.2 nm) purchased from Unidym Inc. were used as received. The polymer Poly(9,9-di-n-dodecylfluorenyl-2,7-diyl) PF12 was solubilized in toluene using a high power ultrasonicator (Misonix 3000) with cup horn bath (output power 69 W) for 20 minutes. Subsequently, SWCNTs were added to form the SWCNT:polymer dispersions with a weight ratio of 1:2 (3mg of SWNTs, 6mg of polymer, 15 ml of toluene). These solutions were then sonicated for 2 h at 69 W and 16 °C.

After ultrasonication, the dispersions were centrifuged at 30 000 rpm (109 000g) for 1 h in an ultracentrifuge (Beckman Coulter Optima XE-90; rotor: SW55Ti) to remove all the remaining nanotube bundles and heavy-weight impurities. After the centrifugation, the highest density components precipitate at the bottom of the centrifugation tube, while the low-density components, including small bundles and individualized SWNTs wrapped by the polymer, and free polymer chains, stay in the upper part as supernatant.

One extra step of ultracentrifugation was implemented to decrease the amount of free polymer in solution (enrichment).[46] For this purpose, the supernatant obtained after the first ultracentrifugation is centrifuged for 5 h at 55 000 rpm (367 000 g). The individualized s-SWNTs are then precipitated to form a pellet and the free polymer is kept in the supernatant. Finally, the pellet is re-dispersed by sonication in toluene.

Deposition of I- capped PbS QDs film. Glass (for the inverters) or n++ Si/SiO_2 (for P(VDF-TrFE-CFE) and P(VDF-TrFE-CFE)/PMMA gate dielectrics comparison) substrates with lithographically patterned silver electrodes were cleaned, after lift-off of the photoresist, with light scrubbing with soap by a latex glove, rinsing and sonication in water, argon plasma treatment, sonication in acetone and, subsequently, isopropanol. Then the substrates were annealed in N_2 filled glovebox before the deposition of the active layer.

Deposition of SWCNT film. Semiconducting SWCNTs were selected by polymer wrapping using the polyfluorene derivative poly(9,9-di-*n*-dodecylfluorenyl-2,7-diyl) (PF12) in toluene using the previously reported method briefly described below.[43] The SWCNTs film was deposited using a blade coating technique inside N_2 filled glovebox. The substrate with previously deposited PbS QDs film covering half of the substrate was placed on a heated (55 °C) surface. 40 µL of a dispersion of SWCNTs (0.5 mg/ml) was dropped in the middle of the substrate, and excess of the solution was removed by a blade, located on 30 µm distance above the surface of the substrate and moving with the velocity of 5 mm/s. The direction of the blade is chosen in a way to deposit the SWCNTs random network on the half of the substrate free from the PbS QDs film. After completing the deposition of both materials, the substrate was annealed for 20 min on a hotplate (120°C) inside the glovebox.

Deposition of P(VDF-TrFE-CFE) and P(VDF-TrFE-CFE) /PMMA. The P(VDF-TrFE-CFE) thin film (~200 nm) was fabricated from a 50 mg/mL P(VDF-TrFE-CFE), VDF:TrFE:CFE = 62.6:29.4:8 solution in cyclohexanone via a two-step spin-coating process. First with the closed spin coater lid at 1400 rpm, with an acceleration of 1000 rpm/s for 90s, followed by an open lid step at 1000 rpm with an acceleration of 1000 rpm/s for 45s. The substrate was then annealed at 120 °C for 20 min to dry the residual cyclohexanone.

For P(VDF-TrFE-CFE) /PMMA film, the PMMA film (~10 nm) was spin-coated (closed lid: 3000 rpm, 3000 rpm/s, 20s) on top of P(VDF-TrFE-CFE) from a 6mg/ml PMMA solution in chloroform.

References

[1] M. J. Speirs, D. N. Dirin, M. Abdu-Aguye, D. M. Balazs, M. V. Kovalenko, M. A. Loi, Energy Environ. Sci. 2016, 9, 2916.

[2] C.-H. M. Chuang, P. R. Brown, V. Bulović, M. G. Bawendi, Nat. Mater. 2014, 13, 796.

[3] L. Sun, J. J. Choi, D. Stachnik, A. C. Bartnik, B.-R. Hyun, G. G. Malliaras, T. Hanrath, F. W. Wise, Nat. Nanotechnol. 2012, 7, 369.

[4] J. Kwak, W. K. Bae, D. Lee, I. Park, J. Lim, M. Park, H. Cho, H. Woo, D. Y. Yoon, K. Char, S. Lee, C. Lee, Nano Lett. 2012, 12, 2362.

[5] T.-H. Kim, K.-S. Cho, E. K. Lee, S. J. Lee, J. Chae, J. W. Kim, D. H. Kim, J.-Y. Kwon, G. Amaratunga, S. Y. Lee, B. L. Choi, Y. Kuk, J. M. Kim, K. Kim, Nat. Photonics 2011, 5, 176.

[6] H. Wang, Z. Li, C. Fu, D. Yang, L. Zhang, S. Yang, B. Zou, IEEE Photonics Technol. Lett. 2015, 27, 612.

[7] L. Mi, Y. Yu, H. Wang, Y. Zhang, X. Yao, Y. Chang, X. Wang, Y. Jiang, Part. Part. Syst. Charact. 2015, 32, 1102.

[8] D. K. Kim, Y. Lai, B. T. Diroll, C. B. Murray, C. R. Kagan, Nat. Commun. 2012, 3, 1216.

[9] W. Koh, S. R. Saudari, A. T. Fafarman, C. R. Kagan, C. B. Murray, Nano Lett. 2011, 11, 4764.

[10] F. S. Stinner, Y. Lai, D. B. Straus, B. T. Diroll, D. K. Kim, C. B. Murray, C. R. Kagan, Nano Lett. 2015, 15, 7155.

[11] M. Jung, J. Kim, J. Noh, N. Lim, C. Lim, G. Lee, J. Kim, H. Kang, K. Jung, A. D. Leonard, J. M. Tour, G. Cho, IEEE Trans. Electron Devices 2010, 57, 571.

[12] T. Takahashi, K. Takei, A. G. Gillies, R. S. Fearing, A. Javey, Nano Lett. 2011, 11, 5408.

[13] C. Wang, D. Hwang, Z. Yu, K. Takei, J. Park, T. Chen, B. Ma, A. Javey, Nat. Mater. 2013, 12, 899.

[14] W. J. Yu, S. H. Chae, S. Y. Lee, D. L. Duong, Y. H. Lee, Adv. Mater. 2011, 23, 1889.

[15] Q. Cao, H. Kim, N. Pimparkar, J. P. Kulkarni, C. Wang, M. Shim, K. Roy, M. A. Alam, J. A. Rogers, Nature 2008, 454, 495.

[16] C. Wang, J. Zhang, C. Zhou, ACS Nano 2010, 4, 7123.

[17] D. Sun, M. Y. Timmermans, Y. Tian, A. G. Nasibulin, E. I. Kauppinen, S. Kishimoto, T. Mizutani, Y. Ohno, Nat. Nanotechnol. 2011, 6, 156.

[18] D. S. Chung, J.-S. Lee, J. Huang, A. Nag, S. Ithurria, D. V. Talapin, Nano Lett. 2012, 12, 1813.

[19] X. Cao, Y. Cao, C. Zhou, ACS Nano 2016, 10, 199.

[20] A. S. Sedra, K. C. Smith, Microelectronic Circuits (The Oxford Series in Electrical and Computer Engineering) 7th Edition, Oxford University Press, 2014.

[21] G. Gelinck, P. Heremans, K. Nomoto, T. D. Anthopoulos, Adv. Mater. 2010, 22, 3778.

[22] C. H. Jo, J. H. Kim, J. Kim, J. Kim, M. S. Oh, M. S. Kang, M.-G. Kim, Y.-H. Kim, B.-K. Ju, S. K. Park, J. Mater. Chem. C 2014, 2, 10305.

[23] W. J. Yu, U. J. Kim, B. R. Kang, I. H. Lee, E.-H. Lee, Y. H. Lee, Nano Lett. 2009, 9, 1401.

[24] B. Kim, M. L. Geier, M. C. Hersam, A. Dodabalapur, ACS Appl. Mater. Interfaces 2015, 7, 27654.

[25] S. G. Bucella, J. M. Salazar-Rios, V. Derenskyi, M. Fritsch, U. Scherf, M. A. Loi, M. Caironi, Adv. Electron. Mater. 2016, 2, 1600094.

[26] G. Li, Q. Li, Y. Jin, Y. Zhao, X. Xiao, K. Jiang, J. Wang, S. Fan, Nanoscale 2015, 7, 17693.

[27] X. Zhang, J. Zhao, J. Dou, M. Tange, W. Xu, L. Mo, J. Xie, W. Xu, C. Ma, T. Okazaki, Z. Cui, Small 2016, 5066.

[28] T.-J. Ha, K. Chen, S. Chuang, K. M. Yu, D. Kiriya, A. Javey, Nano Lett. 2015, 15, 392.

[29] Y. Zhao, Q. Li, X. Xiao, G. Li, Y. Jin, K. Jiang, J. Wang, S. Fan, ACS Nano 2016, 10, 2193.

[30] H. Wang, P. Wei, Y. Li, J. Han, H. R. Lee, B. D. Naab, N. Liu, C. Wang, E. Adijanto, B. C.-K. Tee, S. Morishita, Q. Li, Y. Gao, Y. Cui, Z. Bao, Proc. Natl. Acad. Sci. 2014, 111, 4776.

[31] M. L. Geier, P. L. Prabhumirashi, J. J. McMorrow, W. Xu, J.-W. T. Seo, K. Everaerts, C. H. Kim, T. J. Marks, M. C. Hersam, Nano Lett. 2013, 13, 4810.

[32] J. Huang, S. Somu, A. Busnaina, Nanotechnology 2012, 23, 335203.

[33] W. Honda, T. Arie, S. Akita, K. Takei, Sci. Rep. 2015, 5, 15099.

[34] L. Petti, F. Bottacchi, N. Münzenrieder, H. Faber, G. Cantarella, C. Vogt, L. Büthe, I. Namal, F. Späth, T. Hertel, T. D. Anthopoulos, G. Tröster, in 2014 IEEE Int. Electron Devices Meet., 2014, p. 26.4.1-26.4.4.

[35] P. Vuttipittayamongkol, F. Wu, H. Chen, X. Cao, B. Liu, C. Zhou, Nano Res. 2015, 8, 1159.

[36] B. Kim, S. Jang, M. L. Geier, P. L. Prabhumirashi, M. C. Hersam, A. Dodabalapur, Nano Lett. 2014, 14, 3683.

[37] H. Wang, B. Cobb, A. van Breemen, G. Gelinck, Z. Bao, Adv. Mater. 2014, 26, 4588.

[38] A. G. Shulga, L. Piveteau, S. Z. Bisri, M. V. Kovalenko, M. A. Loi, Adv. Electron. Mater. 2016, 2, 1500467.

[39] S. Wu, M. Shao, Q. Burlingame, X. Chen, M. Lin, K. Xiao, Q. M. Zhang, Appl. Phys. Lett. 2013, 102, 013301.

[40] G. Bertotti, I. D. Mayergoyz, The Science of Hysteresis: Hysteresis in Materials, Gulf Professional Publishing, 2006.

[41] W. Gomulya, V. Derenskyi, E. Kozma, M. Pasini, M. A. Loi, Adv. Funct. Mater. 2015, 25, 5858.

[42] M. Stadermann, S. J. Papadakis, M. R. Falvo, J. Novak, E. Snow, Q. Fu, J. Liu, Y. Fridman, J. J. Boland, R. Superfine, S. Washburn, Phys. Rev. B 2004, 69, 201402.

[43] V. Derenskyi, W. Gomulya, J. M. S. Rios, M. Fritsch, N. Fröhlich, S. Jung, S. Allard, S. Z. Bisri, P. Gordiichuk, A. Herrmann, U. Scherf, M. A. Loi, Adv. Mater. 2014, 26, 5969.

[44] J. R. Hauser, IEEE Trans. Educ. 1993, 36, 363.

[45] M. a. Hines, G. d. Scholes, Adv. Mater. 2003, 15, 1844.

[46] S. Z. Bisri, J. Gao, V. Derenskyi, W. Gomulya, I. Iezhokin, P. Gordiichuk, A. Herrmann, M. A. Loi, Adv. Mater. 2012, 24, 6115.

[47] M. Sytnyk, S. Yakunin, W. Schöfberger, R. T. Lechner, M. Burian, L. Ludescher, N. A. Killilea, A. YousefiAmin, D. Kriegner, J. Stangl, H. Groiss, W. Heiss, ACS Nano 2017, *11*, 1246.

[48] M. Liu, O. Voznyy, R. Sabatini, F. P. García de Arquer, R. Munir, A. H. Balawi, X. Lan, F. Fan, G. Walters, A. R. Kirmani, S. Hoogland, F. Laquai, A. Amassian, E. H. Sargent, Nat. Mater 2017, 16, 258.

[49] V. Derenskyi, W. Gomulya, W. Talsma, J. M. Salazar-Rios, M. Fritsch, P. Nirmalraj, H. Riel, S. Allard, U. Scherf, M. A. Loi, Adv. Mater. 2017, 1606757.

Appendix

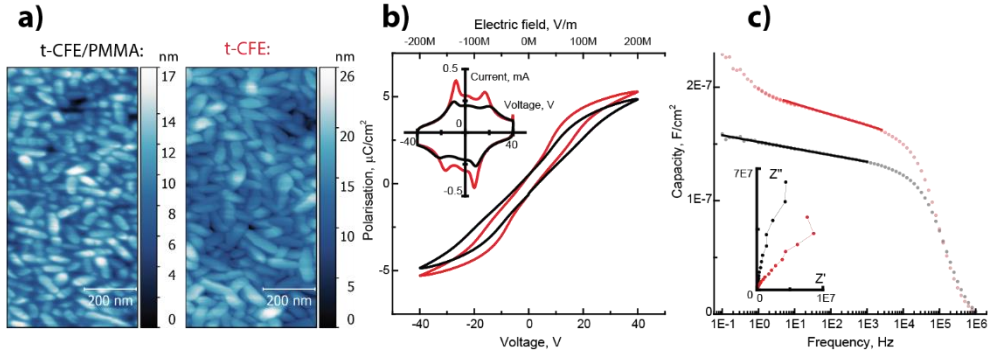
P(VDF-TrFE-CFE)/PMMA dielectric characterization. Appendix Fig. 3A.1 shows the dielectric and ferroelectric properties of capacitors based on a pure P(VDF-TrFE-CFE) thin film and capacitors based on a P(VDF-TrFE-CFE)/PMMA thin film. For both capacitors, spin-coating parameters of P(VDF-TrFE-CFE) solution in cyclohexanone were chosen to obtain a film thickness of 200 nm. For the P(VDF-TrFE-CFE)/PMMA capacitor, a thin layer of PMMA (~10 nm) was spin-casted on top of the P(VDF-TrFE-CFE) film using chloroform as an orthogonal solvent to prevent removal of the P(VDF-TrFE-CFE) layer. The AFM micrographs, depicted in Figure 3.A1a, show no significant difference between the surfaces of the P(VDF-TrFE-CFE) and P(VDF-TrFE-CFE)/PMMA, suggesting that PMMA covers the surface of P(VDF-TrFE-CFE) as a homogeneous thin layer. Thickness measurements done with a Dektak profilometer show that the thickness of the P(VDF-TrFE-CFE)/PMMA film is ~200 nm, which is close to the thickness of the pure t-CFE film. However, Figure 3.A1b shows the reduction of the ferroelectric polarization in the P(VDF-TrFE-CFE)/PMMA compared to the P(VDF-TrFE-CFE) film. The slope of the ferroelectric polarization loop (which is equal to the switching current, see inset) is reduced by the PMMA layer which gives a “tilted” ferroelectric polarization loop. The shape of the polarization loops suggests relaxor ferroelectric nature in both films with a fairly low coercive field.

The impedance spectroscopy (Figure 3.A1c) shows imperfect capacitor behavior of both t-CFE and t-CFE/PMMA films with the capacitance values increasing while decreasing the frequency of the test signal, when described as a parallel connection of an ideal capacitor and an Ohmic resistor. Therefore, the impedance data were more precisely modeled by a constant phase element (CPE) with the impedance defined by equation (1), where Q represents the differential capacitance in the case where $\alpha=1$.

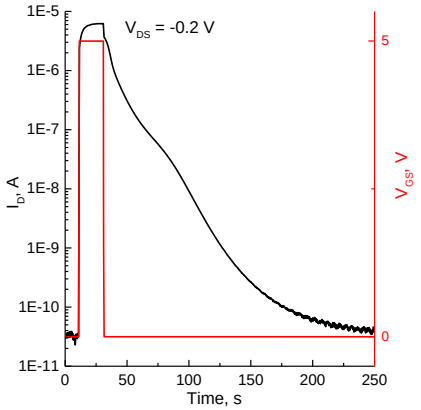
$$Z = \frac{1}{Q(i\omega)^{\alpha}} \quad (1)$$

The experimental data show very good insulating properties of both films (the formation of semicircles in the Nyquist plot, indicating the presence of a parallel

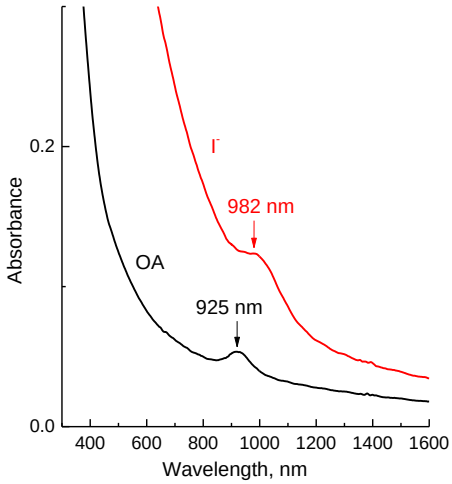
Ohmic resistor, was not observed for the test signal with the frequency down to ν = 0.1 Hz). The extracted α-values (in the frequency ranges indicated in Fig. S1C) for both films are close to the unity (0.977 for the t-CFE, and 0.982 for the t-CFE/PMMA) that justifies the assumption that the Q values are the real differential capacitances of the devices. Therefore, for the t-CFE film, the capacitance is 204 nF·cm^{-2} (k = 46), and for the t-CFE/PMMA film it is 157 nF·cm^{-2} (k = 35), thus decreasing the total capacitance by 23% upon deposition of PMMA. However, it should be noted that some deviation from CPE behavior was observed outside of the frequency ranges used for interpolation. For high frequencies, the parasitic inductivity of the connection probes and cables of the setup may play a role causing the deviation for both films. For low frequencies, in case of the t-CFE film, the capacitance increases even further indicating the decrease of the α with the frequency. The possible explanation is emerging of another process such as the dipoles reorientation a response to the test signal, which is suppressed by the presence of the PMMA layer.



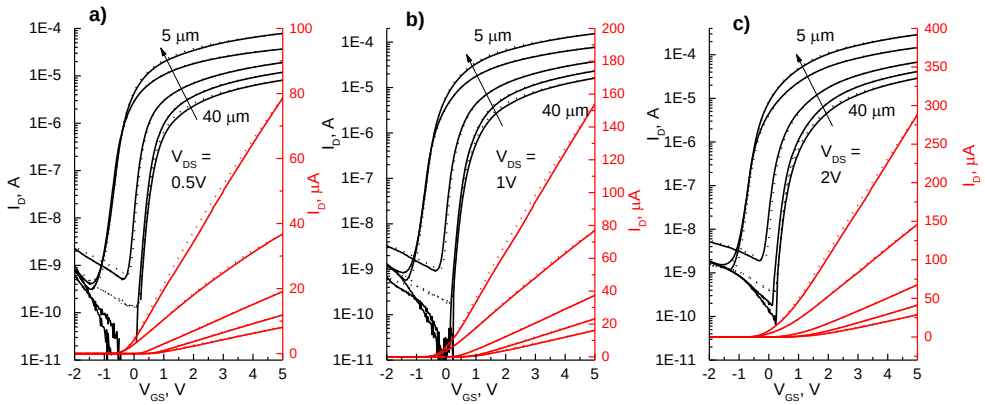
Appendix Figure 3.A1. *Dielectric properties of the P(VDF-TrFE-CFE)/PMMA and P(VDF-TrFE-CFE) thin film capacitors.* ***a)*** *AFM micrographs of the surfaces of the the P(VDF-TrFE-CFE)/PMMA (left) and P(VDF-TrFE-CFE) (right).* ***b)*** *Ferroelectric hysteresis loops of P(VDF-TrFE-CFE)/PMMA (black) and P(VDF-TrFE-CFE) (red). Inset – polarization switching current.* ***c)*** *Impedance measurements of P(VDF-TrFE-CFE)/PMMA (black) and P(VDF-TrFE-CFE) (red) capacitors (circles) with fitting using CPE model (solid lines) in 5 Hz – 2.5 kHz (P(VDF-TrFE-CFE)) and 0.1 Hz – 1 kHz (P(VDF-TrFE-CFE)/PMMA) frequency ranges. Inset –Nyquist plots.*



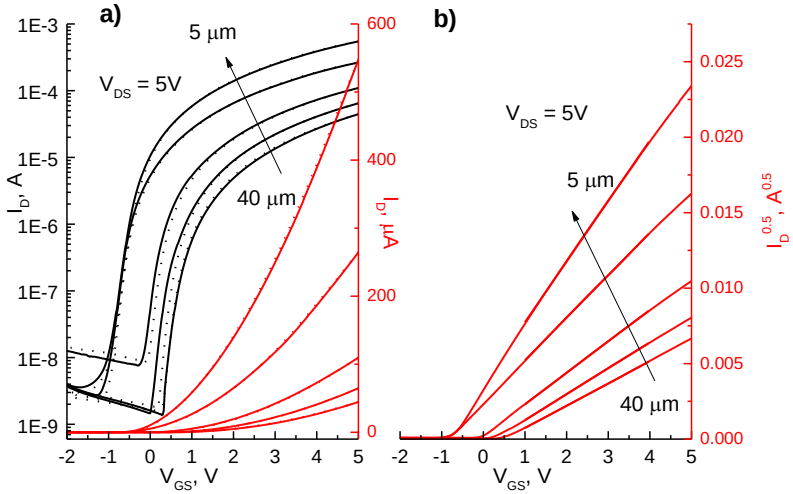
Appendix Figure 3.A2. *Decay of the drain current of t-CFE gated FET after applying the gate voltage pulse for V_{DS} = 0.2 V.*



Appendix Figure 3.A3. *Optical absorbance of OA-capped PbS film (black curve) and I^- capped PbS (red curve).*



Appendix Figure 3.A4. *Transfer curves of t-CFE gated PbS FETs with different channel length (5,10,20,30,40 µm) used for correction the linear mobility for contact resistance for V_{DS} = 0.5V* ***(a)****, V_{DS} = 1V* ***(b)*** *and V_{DS} = 2V* ***(c)*** *in logarithmic (dark curves) and linear (red curves) scale.*



Appendix Figure 3.A5. *Transfer curves of t-CFE gated PbS FETs.* ***a)*** *Transfer curves of t-CFE gated PbS FETs with different channel length (5,10,20,30,40 µm) used for extraction of the saturation mobility (V_{DS} = 5V) in logarithmic (dark curves) and linear (red curves) scale.* ***b)*** *The plot of the square root of the I_D used for linear interpolation for the saturation mobility extraction.*

L, μm	$\mu_{e,\,lin}$, $cm^2V^{-1}s^{-1}$			$\mu_{e,\,sat}$, $cm^2V^{-1}s^{-1}$
	V_{DS} = 0.5V	V_{DS} = 1V	V_{DS} = 2V	
5	0.18	0.19	0.20	0.21
10	0.15	0.18	0.20	0.2
20	0.20	0.21	0.22	0.22
30	0.20	0.22	0.22	0.23
40	0.19	0.21	0.22	0.22

Appendix Table 3.A1. *Linear and saturation electron mobility of I^- capped PbS FETs with different channel length.*

V_{DS},V	$\mu_{e\,CR}$, $cm^2V^{-1}s^{-1}$	$R_C\cdot(V_{GS}-V_T)$, kΩ·V
0.5	0.19	9.9
1	0.21	8.0
2	0.22	5.3

Appendix Table 3.A2. *Linear and electron mobility after the correction for contact resistance and $R_C\cdot(V_{GS}-V_T)$ of I^- capped PbS FETs for different V_{DS}. The correction was made using the relationship $I_D = \mu_{e\,CR}C_{OX}WL^{-1}(V_{GS}-V_T)(V_{DS}-I_DR_C)$ and the curves shown in Fig. 3.A3.*